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Specification

1. Title of the Invention

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

2. Scope of Patent claims

1) A method of manufacturing a semiconductor device, characterized in that a gate insulating film of an insulating gate type field effect transistor is formed by a plasma CVD method using a monosilane derivative gas including at least one of chlorine and fluorine.

2) A method of manufacturing a semiconductor device, characterized in that a gate insulating film of an insulating gate type field effect transistor is formed by a plasma CVD method using at least hydrogen chloride.

3) A method of manufacturing a semiconductor device according to claim 1 or 2, wherein at least one portion of a channel area of said insulating gate type transistor is a non-monocrystal semiconductor.

3. Detailed Description of the Invention

[Field of the Industrial Application]

The present invention relates to a method of manufacturing a semiconductor device, and particularly relates to a forming method of a gate insulating film of an insulating gate type field effect transistor.

[Prior Art]

In recent years, as needs for a three-dimensional IC, a large-sized liquid crystal display panel with high resolution, a close type image sensor with high resolution operated at high speed, etc. are increased, a technique for forming a gate insulating film with a good quality at a low temperature has become important. A thermal oxidation method uses a high temperature process at about 900 to 1200°C. Therefore, there are problems in that (1) no element can be formed on a cheap glass substrate, (2) the thermal oxidation method has a bad influence (redistribution of impurities, etc.) on an element of a lower layer portion in the three-dimensional IC, etc. Accordingly, a technique for forming an oxide film at a low temperature by the CVD method, etc. is considered.

[Problems to be solved by the Invention]

However, in the oxide film formed by the conventional CVD method, there is a problem in that gate insulation resisting

voltage is low and interface level density is high, etc. Accordingly, it has been difficult to stably form an element at a practical level. To solve such a problem, an object of the present invention is to provide a method of forming a gate insulating film for an insulating gate type field effect transistor in which gate insulation resisting voltage is high and interface level density is low.

[Means for solving the Problems]

A method of manufacturing a semiconductor device according to the present invention is characterized in that a gate insulating film of an insulating gate type field effect transistor is formed by the plasma CVD method using a monosilane derivative gas including at least one of chlorine and fluorine.

Further, a method of manufacturing a semiconductor device according to the present invention is characterized in that a gate insulating film of an insulating gate type field effect transistor is formed by the plasma CVD method using at least hydrogen chloride.

[Example]

Fig. 1 shows one example of a manufacturing process view of a semiconductor device in an embodiment of the present invention. In the example of Fig. 1, a thin film transistor (TFT) is formed as a semiconductor element.

Fig. 1(a) shows a process for forming a silicon layer 102 on an insulating amorphous substrate of glass, quartz, etc., or an insulating amorphous material 101 such as an insulating amorphous material layer of SiO_2, etc. In one example of a film forming condition, there is a method for forming a silicon film having about 100 Å to 2000 Å in film thickness at about 500°C to 560°C by the LPCVD method, etc. There is also a method in which the substrate is held at a temperature from a room temperature to about 800°C by the plasma CVD method, monosilane or a gas obtained by diluting monosilane with hydrogen, argon, helium, etc. is introduced into a reaction chamber, and is decomposed by applying high frequency energy, etc., and a silicon layer having about 100 Å to 2000 Å in film thickness is formed on a desirable substrate. However, the film forming method is not limited to these methods. For example, there are methods of forming amorphous silicon or fine crystal silicon by the sputtering method, the evaporation method, the EB evaporation method, the MBE method, etc.

Fig. 1(b) shows a process for crystal-growing the silicon layer 102 by heat treatment, etc. An optimal condition of a heat treatment condition differs in accordance with the film forming method of the silicon layer in the process (a).

For example, when the silicon layer is formed by the LPCVD method, a polycrystal silicon layer 103 is formed by

performing the heat treatment at about 550°C to 650°C for about 2 to 50 hours within the atmosphere of an inert gas such as nitrogen or argon (Ar), etc.

For example, when the silicon layer is formed by the plasma CVD method, the following differences exist in accordance with the substrate temperature at a film forming time.

(1) A film formed at a relatively low substrate temperature from the room temperature to about 150°C becomes amorphous silicon including a large amount of hydrogen in the film. However, hydrogen within the film can be removed therefrom by the heat treatment at a lower temperature in comparison with a film formed at about 200 to 300°C. One example of the heat treatment condition will next be described. A first anneal is performed with respect to the amorphous silicon film after this film is formed within the plasma CVD reaction chamber. The amorphous silicon film formed at a low film forming temperature is a porous film. Therefore, when the silicon film is taken out into the atmosphere as it is after the film formation, oxygen, etc. tend to be taken into this film and cause a reduction in film quality. However, when suitable heat treatment is performed before the taking-out into the atmosphere, the silicon film is closely formed, and the taking-in of oxygen, etc. is prevented. The heat treatment

temperature is desirably set to 300°C or more. A large effect is particularly obtained when the heat treatment temperature is raised up to about 400 to 500°C. The effect of closeness of the film using the heat treatment exists even when the heat treatment temperature is lower than 300°C. However, when the anneal is continuously performed without breaking a vacuum, the first anneal can be also omitted.

Subsequently, a second anneal is performed. When the heat treatment at a relatively low temperature of about 550°C to 650°C is performed for about several hours to 40 hours with respect to the amorphous silicon film formed at a low film forming temperature, hydrogen is separated from the silicon film and crystal growth is caused. Thus, polycrystal silicon having a large crystal particle diameter of about 1 to 2 μm is formed. In each of the first anneal and the second anneal, it is not preferable to suddenly increase the film temperature in a short time when the film temperature is raised up to a predetermined anneal temperature. This is because hydrogen within the silicon film is separated therefrom as the film temperature rises (when the film temperature particularly exceeds 300°C), and a defect is easily formed in the silicon film at a sudden temperature rising speed. There are also cases in which a pinhole is formed and the silicon film is separated. The defect in the silicon film is reduced when the

film temperature is gradually raised at a temperature rising speed slower than 20°C/minute (the temperature rising speed slower than 5°C/minute is particularly desirable) at a temperature equal to or higher than at least 300°C. A temperature raising method will be described later in detail.

(2) In the silicon film formed at a substrate temperature of about 150°C to 300°C, a hydrogen amount within the film is reduced, but a separating temperature of hydrogen is shifted to a higher temperature side in comparison with the amorphous silicon film formed at the above low temperature. Since the formed film is closer than a film formed at low temperature, the above first anneal can be also omitted. In a second anneal condition, when the heat treatment is performed for several hours to 40 hours at about 550°C to 650°C, hydrogen separation and crystal growth are caused, and polycrystal silicon having a large crystal particle diameter of from 1 to 2 μm is formed. A detailed temperature raising method from 550°C to 650°C will be described later. However, similarly to the case of (1), at a temperature equal to or higher than at least 300°C, it is desirable to gradually increase the substrate temperature at a temperature rising speed slower than 20°C/minute (desirably, 5°C/minute) since the defect in the silicon film is reduced.

(3) When the substrate temperature exceeds 300°C, the

hydrogen amount within the silicon film is further reduced. However, hydrogen is easily separated in the anneal at a temperature of about 550°C to 650°C so that the heat treatment at a temperature higher than the above temperature becomes important. When a film formed at a substrate temperature of about 500°C or more is grown in solid phase, polycrystal silicon oriented to <110> or <100> is obtained. Therefore, there are effects of a reduction in interface level density of the TFT, an improvement of electric field effect mobility, etc.

Fig. 1(c) shows a process for thermally processing the polycrystal silicon layer 103 at a predetermined heat treatment temperature higher than that in the process (b). The process (c) can be also omitted, but is an important process to improve crystallization ratio. The crystallization ratio of the polycrystal silicon layer 103 crystal-grown by a solid phase growing method in the process (b) is not necessarily high. In particular, when a silicon film (amorphous silicon or fine crystal silicon having a fine crystal area within an amorphous phase is formed) formed at a relatively low temperature of about 500°C to 560°C by the LPCVD method is grown in solid phase by the heat treatment, its crystallization ratio is a low ratio such as about 50% to 70%. Therefore, it is important to arrange a process for crystallizing an uncrystallizing area of the polycrystal

silicon layer by performing the heat treatment in the process (c) at a temperature higher than that in the process (b). As a result, the crystallization ratio can be increased to 99% or more. An optimal value of the heat treatment temperature lies approximately between 700°C and 1200°C. However, when glass is used as the substrate, no glass can be exposed to the above high temperature. Therefore, it is important to increase only a portion near the surface layer of a semiconductor up to the above temperature by irradiating short wavelength light such as an excimer laser, and optimize irradiating strength and an irradiating time such that the semiconductor layer and a portion near a substrate interface are equal to or lower than about 800°C. In one example, the above condition is satisfied when an XaCl excimer laser (wavelength of 308 nm) is used, and 1 to 10 pulses (several tens of ns per one pulse) are irradiated with irradiating intensity of about 0.1 to 1.0 J/cm^2, etc. If the interface of the semiconductor layer and the substrate is equal to or lower than about 600°C in the irradiation of a laser beam, it is preferable to melt the surface of the semiconductor layer since crystallization property of the semiconductor surface layer becomes preferable. In particular, since the surface layer is an area for forming an inverting layer, transistor characteristics are improved by improving the crystallization property of the surface layer.

As another heat treatment method, there is a method of performing the heat treatment for e.g., about one hour at 850°C, or about 10 to 20 minutes at 1000°C within the atmosphere of an inert gas such as nitrogen or Ar, etc. in an anneal furnace. There are also a method of lamp anneal using a halogen lamp, an arc lamp, an infrared lamp, a xenon lamp, a mercury lamp, etc., a method of laser anneal using an Ar laser, a He-Ne laser, etc., and the like.

Fig. 1(d) shows a process for forming a gate insulating film 104 by the plasma CVD method using a monosilane derivative gas including at least one of chlorine and fluorine. In an oxide film formed by the conventional normal pressure CVD method, insulation-resisting voltage is low, interface level density of Si/SiO_2 is high, and no oxide film at a practical level can be stably formed. However, as a result of our consideration, it has become clear that the oxide film of good quality can be formed at a low temperature by forming this film by the plasma CVD method using the monosilane derivative gas such as dichlorosilane, etc. including at least one element among chlorine and fluorine. In one example of the film forming method, there is a method in which dichlorosilane (SiH_2Cl_2) and oxygen or nitrous oxide (N_2O) are introduced to a plasma CVD device as a reaction gas, the substrate temperature is held at about 200°C to 450°C, and this gas is decomposed by

applying a high frequency wave so that an oxide film is formed, etc. A monosilane derivative gas including at least one element among chlorine and fluorine such as monochlorosilane (SiH_3Cl), silane trichloride ($SiHCl_3$), silicon tetrachloride ($SiCl_4$), monofluorosilane (SiH_2F), difluorosilane (SiH_2F_2), trifluorosilane ($SiHF_2$), silicon tetrafluoride (SiF_4), etc. may be also used instead of dichlorosilane. Plural gases among these gases may be mixed and used, and monosilane and these gases may be also mixed and used. Similar effects are obtained even when the oxide film is formed by mixing hydrogen chloride (HCl) with monosilane or the monosilane derivative gas. When monosilane is mixed with the monosilane derivative gas of dichlorosilane, etc. or hydrogen chloride, etc., it is also effective to use a method for changing a ratio of this mixture with the passage of time. Namely, there is a method for increasing the ratio of monosilane with the passage of time, etc. by increasing the ratio of the monosilane derivative gas of dichlorosilane, etc. or hydrogen chloride at a starting time of the film formation. In this method, there are effects in that insulation resisting voltage is increased and interface level density is reduced. The reasons for this are guessed as follows. Since the ratio of the monosilane derivative gas including an element such as chlorine or fluorine, etc., or hydrogen chloride is increased at the film

forming time, the interface level density can be reduced by forming the oxide film while a natural oxide film and a polluted substance of an organic substance, a metal, etc. on the silicon layer 102 are removed. Subsequently, the amounts of chlorine and fluorine mixed into the oxide film are reduced by increasing the ratio of monosilane gas, and the oxide film with high insulation resisting voltage and good quality can be formed. Figs. 2(a) and 2(b) schematically show time charts of gas flow rates. In Fig. 2, reference numerals 201 and 202 respectively designate the flow rate of monosilane gas and the flow rate of dichlorosilane gas. Fig. 2(a) shows a case in which dichlorosilane is set to 100% at the starting time of the film formation, and the flow rate of dichlorosilane is reduced and the flow rate of monosilane is increased with the passage of time. Fig. 2(b) shows a case in which the gas flow rates are stepwise changed. The time charts of the gas flow rates are not limited to Fig. 2, but it is important to increase the ratio of the silane derivative gas of dichlorosilane, etc., or hydrogen chloride, etc. at the starting time of the film formation.

Fig. 1(e) shows a process for forming a semiconductor element. Fig. 1(e) shows an example in which a TFT is formed as the semiconductor element. In this figure, reference numerals 104, 105 and 106 respectively show a gate insulating

film, a gate electrode and a source-drain area. Reference numerals 107, 108 and 109 respectively designate an interlayer insulating film, a contact hole and wiring. In one example of a TFT forming method, the source-drain area is formed by the ion injecting method, the heat diffusion method, the plasma doping method, the ion shower doping method, etc. after the gate electrode is formed. The interlayer insulating film is formed by the CVD method, the sputtering method, the plasma CVD method, etc. Further, the contact hole is bored in the interlayer insulating film, and the wiring is formed so that the TFT is formed. In the forming method of the source-drain area using glass as a substrate, impurities of B, P, etc. are implanted by the ion injecting method, and are then thermally processed for several hours to several tens of hours at a low temperature of about 600°C so that these impurities are activated. Further, the ion shower doping method, the plasma doping method, etc. are effective.

In the present invention, it is important that the oxide film of good quality can be formed at low temperature by the plasma CVD method instead of the conventional thermal oxidation method and the conventional CVD method. These contents will next be described in detail. In the conventional CVD method, the insulation resisting voltage is low and the Si/SiO_2 interface level density is high and no oxide film at a

practical level can be stably formed as mentioned above. In the thermal oxidation method, there are problems that a high temperature process at about 900°C to 1200°C is used, and that the insulation resisting voltage is as low as about 3 to 4 MV/cm on polycrystal silicon. However, it has become clear that the insulation resisting voltage of the oxide film formed by the plasma CVD method of the present invention is improved in comparison with a film formed by the thermal oxidation method, and is about 7 to 8 MV/cm. The reasons for this are as follows. When polycrystal silicon is thermally oxidized, oxidation is easily advanced along a crystal grain boundary so that the oxide film is formed in a projection shape and electric field concentration is easily caused. In contrast to this, when the oxide film is formed at a low temperature by the plasma CVD method, no oxygen is almost diffused along the crystal grain boundary, and the above electric field concentration is not easily caused. Therefore, it is considered that the insulation resisting voltage is improved. Further, a high electric potential barrier is formed in a crystal grain boundary portion by the oxidation along the crystal grain boundary so that electric field effect mobility of the TFT is reduced. However, when the oxide film of the present invention is used, there are also effects in that there is almost no diffusion of oxygen along the crystal grain

boundary portion, and the electric potential barrier of the crystal grain boundary portion can be reduced so that the electric field effect mobility is greatly improved. Further, it is also important that the interface level density can be reduced by forming the oxide film by using the silane derivative gas of dichlorosilane, etc., or hydrogen chloride, etc. while the natural oxide film and the polluted substance of an organic substance, a metal, etc. on the silicon layer 102 are removed.

The oxide film using the plasma CVD method based on the present invention can be formed at a low temperature equal to or lower than about 450°C. Therefore, this oxide film can be also applied to a low temperature process using a cheap glass substrate.

In the embodiment of Fig. 1, the oxide film is formed by the plasma CVD method using the silane derivative gas of dichlorosilane, etc. However, the present invention is not limited to this case. The oxide film with high insulation resisting voltage and low interface level density can be also formed very effectively even when the oxide film is formed by using the above gas in the CVD method, the ECR-plasma CVD method, the optical CVD method, etc.

The electric field effect mobility of a polycrystal silicon TFT (N-channel) formed in the low temperature process

using the method of manufacturing a semiconductor device based on the present invention approximately ranges from 150 to 200 $cm^2/V \cdot sec$, and excellent characteristics are obtained in comparison with the TFT formed by the thermal oxidation method.

Further, when a process for exposing a semiconductor element to the plasma atmosphere of a gas including at least hydrogen gas or ammonia gas in the above TFT manufacturing process, etc. are arranged and the above TFT is hydrogenated, defective density existing in the crystal grain boundary is reduced and the above electric field effect mobility is further improved.

It is also very effective to use a means for controlling a threshold voltage value Vth by doping impurities to a channel area. In the polycrystal silicon TFT formed by the solid phase growing method, the threshold voltage Vth of an N-channel transistor tends to be shifted in a depression direction, and the threshold voltage Vth of a P-channel transistor tends to be shifted in an enhancement direction. When the above TFT is hydrogenated, this tendency becomes more notable. Therefore, when impurities of about 10^{15} to $10^{19}/cm^3$ are doped to the channel area, the shift of the threshold voltage Vth can be restrained. For example, in Fig. 1, there is a method in which the impurities such as B (boron) having a dose amount of about 10^{11} to $10^{13}/cm^3$ are implanted by the ion

injecting method, etc. before the gate electrode is formed. In particular, if the dose amount is approximately equal to the above value, the threshold voltage Vth can be controlled such that an off-state current is minimized in both the P-channel transistor and the N-channel transistor. Accordingly, when the TFT element of a CMOS type is formed, an entire face can be also channel-doped in the same process without selectively channel-doping the P-channel and the N-channel.

As shown in the embodiment of Fig. 1, the present invention has a great merit in that the polysilicon TFT of high performance can be formed at a low temperature. However, the present invention is not limited to this case. The present invention becomes a very effective manufacturing method when a gate insulating film on monocrystal silicon, a gate insulating film on non-monocrystal silicon such as polycrystal silicon, fine crystal silicon, amorphous silicon, etc. are formed at a low temperature. Furthermore, the present invention is not limited to the TFT, but can be generally applied to an insulating gate type semiconductor element. Further, the oxide film of the present invention can be also used in an interlayer insulating film, a passivation film, etc. in addition to the gate insulating film, and has a great merit in that the insulating film of high insulation resisting voltage can be formed at a low temperature.

[Effect of the Invention]

As mentioned above, in accordance with the present invention, the oxide film of high insulation resisting voltage and low interface level density can be formed at a low temperature. In particular, when the oxide film is formed on polycrystal silicon by the plasma CVD method of the present invention, the insulation resisting voltage can be increased and the interface level density can be reduced in comparison with a case in which the oxide film is formed by thermally oxidizing polycrystal silicon. Further, there is also an effect in that electric field effect mobility of the TFT is greatly improved in comparison with the thermal oxidation film. As a result, the semiconductor element of high performance can be formed on an insulating amorphous material, and it is possible to easily form a large-sized liquid crystal display panel with high resolution, and a close type image sensor and a three-dimensional IC, etc. with high resolution operated at high speed. In the forming method of the oxide film of the present invention, the low temperature process is used so that a cheap glass substrate can be also used as a substrate. In the three-dimensional IC, an element of an upper layer portion can be also formed without having any bad influence (for example, redistribution of impurities, etc.) on an element of a lower layer portion.

Further, the present invention can be also generally applied to an insulating gate type semiconductor element in addition to the TFT shown in the embodiment of Fig. 1.

4. Brief Description of the Drawings

Figs. 1(a) to 1(e) are manufacturing process views of a semiconductor device in an embodiment of the present invention.

Figs. 2(a) and 2(b) are schematic time charts of gas flow rates.

101 --- insulating amorphous material

102 --- silicon layer

103 --- polycrystal silicon layer

104 --- gate insulating film

105 --- gate electrode

106 --- source-drain area

107 --- interlayer insulating film

108 --- contact hole

109 --- wiring

201 --- flow rate of monosilane

202 --- flow rate of dichlorosilane

DRAWINGS

FIG. 1

103' CRYSTAL GRAIN BOUNDARY

FIG. 2(a)

GAS FLOW RATE

DEPOSITION TERMINATION

TIME